UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,934	07/07/2003	Takehiro Shimizu	H-1098	6928

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EXAMINER
JOHNSON, BRIAN P

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

	Application No.	Applicant(s)
Office Action Summary	10/612,934	SHIMIZU ET AL.
	Examiner	**Art Unit**	
	Brian P. Johnson	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>06 March 2007</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,8 and 9* is/are pending in the application.

　　4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1, 8, and 9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

　　Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

　　Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

　　a)☐ All　b)☐ Some * c)☐ None of:

　　　1.☐ Certified copies of the priority documents have been received.

　　　2.☐ Certified copies of the priority documents have been received in Application No. _____.

　　　3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

　　* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
　　Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
　　Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

1.   Claims 1, 8, and 9 have been examined.

2.   Acknowledgement of papers filed: RCE and amendments filed 6 March 2007.

These papers filed have been placed on record.

Specification

3.   Title is accepted. Objection is withdrawn.

Claim Rejections - 35 USC § 112

4.   Rejection of claim 12 has been rendered moot in view of its cancellation.

Claim Rejections - 35 USC § 102

5.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6.   Claims 1, 8, and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by

Talcott (U.S. Patent No. 5,964,869).

Regarding claim 1, Talcott discloses a data processing device which decodes

(col 5 lines 39-40) and executes instructions (col 5 lines 62-64) of a predetermined

length instruction set (col 11 lines 26-30) containing a spare field (TBAT reference 208), comprising:

An instruction cache memory (col 5 line 39).

A predecode-processor (col 8 lines 8-13) which decodes operation codes contained in first fields of each of said instructions to generate a piece of information (col 8 lines 8-13), said information representing whether said instruction is a branch instruction or not (col 8 lines 11-13), and sets information in said spare field of each of said instructions (col 11 lines 10-14);

Note that the one-to-one correspondence allows the predecode bits to be a portion of the instruction or "spare field".

Wherein the instruction cache memory holds the information in said spare field of each of said instructions (col 11 lines 26-30),

An instruction flow unit which controls an executing sequence of said instructions based on information of said spare field, when executing instructions loaded from said cache memory (col 3 lines 35-49),

Wherein the instruction flow unit issues commands to fetch an instruction of a branch destination, when it determines that said instruction is a branch instruction according to said information of the said spare field (col 8 lines 8-13), and

Wherein the spare field is a reserved field or an open field in the instructions of said predetermined length instruction set (col 11 lines 26-30).

7.   Regarding claim 8, Talcott discloses the data processing device according to

claim 1, wherein the instruction flow comprises:

A queuing buffer temporarily storing instructions loaded from said instruction

cache memory (col 8 lines 3-7); and

A target buffer which holds an address of said branch destination (col 3 lines 41-

45), said instruction of said address of said branch destination (col 4 lines 61-62),

Note that the elements of memory that contain this information are considered to

be the "target buffer".

Wherein said instruction flow unit divides one branch operation into a prepare

target instruction and a branch procedure instruction (see below),

Wherein said prepare target instruction commands calculating of said address of

said branch destination and fetching of said instruction of said branch destination (col 3

lines 41-45),

Wherein said branch procedure instruction commands branch condition checks

and branch procedures (col 5 lines 58-62).

Note that the Computer Science definition of the American Heritage College

Dictionary, 4th Edition states that an instruction is "a sequence of bits that tells a central

processing unit to perform a particular operation and can contain data to be used in that

operation". The branch instruction completes both the operations of the "branch

procedure instruction" and the "prepare target instruction"; therefore, it is considered to

be split into those instructions.

8.   Regarding claim 9, Talcott discloses the data processing device according to

claim 8, wherein said instruction flow unit issues commands to load said instruction of

said branch destination and said following address from said target buffer when said

instruction flow unit determines that said instruction is a branch procedure instruction

according to said information of said queuing buffer (col 5 lines 52-57).

Response to Arguments

9.   Applicant's arguments filed 6 March 2007 regarding Talcott have been fully

considered but they are not persuasive.'

10.   Applicant's arguments with regard to Augsberg have been found persuasive.

Consequently, these rejections have been withdrawn.

11.   Applicant states:

> "Talcott does not teach or suggest where the instruction cache memory holds the information in
> the spare field of each of the instructions, in the mnner claimed. In the present invention, the instruction
> cache memory holds the information in the spare field, where the information represents whether or not
> the instruction is a branch instruction or not, and where the spare field is a reserved field or an open field
> in the instruction of predetermined length instruction. This structure does not need to increase the
> capacity of the instruction cache because of the use of the spare field to temporarily store information of
> various types in that field. To the contrary, Talcott needs an extra memory device or memory area (see,
> e.g., the TBAT 208 and column 8, line 8-23). Therefore, Talcott does not disclose the use of a spare field
> in the instructions of predetermined length instruction set, as in the present invention."

Examiner disagreed. Talcott's storing of the predecode bits does not cause the

instruction length to vary. Col. 11 lines 26-30 states: "In one embodiment, the

predecode tag data stored in TBAT 208 is redundant with the predecode tag data stored

in the instruction storage 222. The predecode tag data is stored in TBAT 208 to expedite access to the predecode data."

It is clear from this situation that, at least in the embodiment described, the predecode bits are not additional or extending bits of certain instructions, but standard fields used for all instructions and stored in the TBAT to expedite processing.

Applicant further states:

"For example, Talcott does not teach or suggest where the spare field is a reserved field or an opened field in the instructions of the predetermined length instruction set, as in the present invention."

Again, Examiner disagrees. The predecode data is a standard field within the instruction storage 222 for a predetermined length instruction set. This field is specifically reserved for the predecode bits.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

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For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

RICHARD L. ELLIS
PRIMARY EXAMINER